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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,918	05/31/2001	Neal T. Wingen	VLSI.316PA	7781

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EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	6

DATE MAILED: 05/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/870,918	WINGEN, NEAL T.
	Examiner	Art Unit
	Nitin C. Patel	2116

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-10 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-10 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 28 January 2002 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 10 are presented for examination.

Specification

2. The abstract of the disclosure is objected to because on page 6, line 19 replace the word "deactivating (TL)" --- with ---deactivating (TL1)---. Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because of the following informalities:

In the specification:

on page 6, line 19 replaces the word "deactivating (TL)" --- with ---deactivating (TL1)--- as no reference for TL in drawings.

on page 8, line 2 replace the numeral "104" after interrupt control circuit with ---106---as shown in fig. 2.

Appropriate correction is required.

Drawings

4. The drawings are objected to because in fig. 1 two different inputs [TL1, TL2] received at different ports with same numerals as CLK2. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson, US Patent 5,661,751, and further in view of Wegner et al. [hereinafter as Wagner], US Patent 5,649,122.

8. As to claim 1, Johnson teaches system and method for power management of a universal asynchronous receiver/transmitter [UART] with an arrangement of plurality of integrated circuit devices [fig.1] with parallel data bus [CPU interface] to communicate with first integrated circuit [CPU] in response to first clock [system clock is inherent to CPU], a UART [108] including a serial communication circuit [112, transmit state machine, 114, receive state machine] adapted to communicate serial data at a second rate defined by second clock [122, clock divider output], a parallel bus interface circuit [transmit and receive FIFO] adapted to pass data between the parallel bus and serial communication circuit [112, 114] and a clock control circuit with synchronous clock gate [102, 104] to assert a clock enable signal by detecting various predetermined system activities associated with UART which, allows the baud rate signal to be generated otherwise no UART clock at line 122 and as a result of this overall power consumption is decreased when UART is idle [col. 3, lines 51 – 67, col. 4, lines 1 – 67, fig. 1].

However, Johnson's clock control circuit does not teach explicitly to reduce the first clock rate in response to clock control signal and provide a power-reduced UART mode in which serial communication is continue communication at the second rate.

Wegner teaches UART device with a clock control circuit [600, fig. 6] with a frequency divisor [602], multiplexer [MUX] [603] with clock input at one input of MUX [A] and divisor out at other input of MUX [B] and select signal at select input of MUX [SEL B] and output of MUX [OUT] to baud rate generator of UART which output as a clock input [first clock] or a divisor out [second clock] depending on selection input [power mode] and provided to baud rate generator [col. 7, lines 21 – 61, fig. 6]. Therefore, Wegner teaches reducing of a first clock rate in response to clock control signal and providing a power-reduced UART mode in which serial communication is continue communication at second rate.

It would have been an obvious to one of an ordinary skill in the art at the time of the claimed invention to combine the teachings of Johnson and Wegner because both are commonly directed to clock control during a power-reduced mode UART in data communication, and Wegner's clock rate reducing responsive to control signal provide a power-reduced UART mode, when incorporated into Johnson, would have enabled power saving and enhanced user flexibility [abstract].

9. As to claim 2, Johnson teaches the clock control circuit to reduce the first clock rate to zero [clock is disabled when UART is idle][col. 2, lines 11 – 13].

10. As to claim 3, Wagner teaches to reduce the first clock rate that is at least ten percent slower than the first clock [it is inherent to frequency division circuit to get desired frequency by selecting a corresponding divisor value] [fig. 6].

11. As to claim 4, Johnson teaches to derive a second clock rate [122] from the first clock rate [136] [fig. 1].

12. As to claim 5, Johnson teaches a first clock rate and second clock rate change states asynchronously [as first clock rate and second clock rate change states in responsive to the control signal, fig. 1].

13. As to claim 6, Johnson teaches that the second clock rate [122] is set to define serial communication with another of the plurality of integrated devices [fig. 1].

14. As to claims 7, and 8, Johnson teaches the UART chip including first-in-first-out [FIFO] buffers [transmit and receive FIFO] to store data passing between the serial communication circuit and the parallel bus interface circuit, and data-storage-register [holding and buffer register] to provide flow condition for data [col. 3, lines 57 – 64, col. 4, lines 15 – 40, col. 6, lines 30 – 38, fig. 1].

15. As to claims 9, and 10, Wegner teaches a logic circuit for software flow control with the use of different registers [RHR, THR, IER, FCR, ISR, LCR, MCR, SCR][col. 1, lines 54 – 56, col. 5, lines 8 – 67, col. 9, lines 20 – 65, col. 10, lines 8 – 63, fig. 8a-8b].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 703-305-3994. The examiner can normally be reached on 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Brown can be reached on 703-308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
May 13, 2004

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